A 48-Gb/s Baud-Rate PAM-4 Receiver Using Modified Time-Interpolated Latches

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***Abstract*—This brief presents a 48-Gb/s quarter-rate four-level pulse amplitude modulation (PAM-4) receiver with a baud-rate clock and data recovery circuit. The modified time-interpolated latch (MTIL) is proposed to reduce the number of input comparators. The offset voltages of the comparators and the intersecting voltages of the MTILs are calibrated by using the foreground calibration. This PAM-4 receiver is fabricated in a 40-nm CMOS process and the active area is 0.089mm^2. The power consumption is 62.8mW and the calculated energy efficiency is 1.31pJ/b. For a PRBS of 2^7-1, the bit-error rate is less than 10^{-12}.**

***Index Terms*—Four-level pulse amplitude modulation, clock and data recovery, phase detector, continuous-time linear equalizer, time-interpolated latch.**

I. Introduction

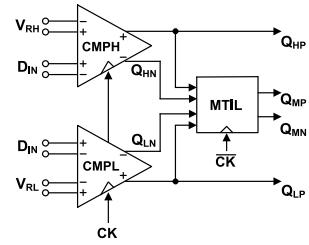
THE DEMAND for the high-speed data transmission in modern wireline communication systems is increasing. Four-level pulse-amplitude modulation (PAM-4) signaling is attractive due to its better bandwidth efficiency [1], compared to non-return-to-zero (NRZ) signaling. A quarter-rate PAM-4 receiver with a baud-rate clock and data recovery (CDR) circuit needs several comparators to recover the data and compare the phase error [1], [2], [3], [4], [5]. These comparators not only increase the power consumption but also increase the capacitive loadings for the preceding continuous-time linear equalizer (CTLE). In [3], the time-based technique is presented to reduce the number of input comparators in the PAM-4 receiver. However, [3] didn't realize the CDR circuit. In [4], a quarter-rate PAM-4 receiver using the baud-rate technique is presented to enhance the power efficiency. However, it requires 20 comparators to complete the phase detection and data recovery. In [5], a quarter-rate PAM-4 receiver using time-interpolated latches [6], [7] is presented, which needs 16 comparators.

In this brief, a quarter-rate PAM-4 receiver with a baud-rate CDR circuit is presented. The baud-rate phase detector (PD) [8], [9] is utilized to reduce the number of the multiple-phase clocks and their buffers. To further reduce the number of input comparators, a modified time-interpolated latch (MTIL) is presented. By using the proposed MTILs, only 8 comparators are needed for a quarter-rate PAM-4 receiver with the baud-rate CDR circuit. Table I summarizes the number of comparators and the sampling techniques among the prior art [4], [5], [10] and this brief.

This brief is organized as follows. Section II presents the analog front-end of the PAM-4 receiver. Section III gives the circuit description. The experimental results are given in Section IV. Finally, the conclusion is given in Section V.

TABLE I
COMPARISON OF QUARTER-RATE PAM-4 RECEIVERS

	[4]	[5]	[10]	Proposed
Sampling tech.	Baud-rate	Baud-rate	Oversampling	Baud-rate
# of Comp.	20	16	16	8



(a)

Region	Q_{HP}	Q_{HN}	Q_{LP}	Q_{LN}
$D_{IN}>V_{RH}$	1	0	1	0
$V_{RH}>D_{IN}>V_{RL}$	0	1	1	0
$V_{RL}>D_{IN}$	0	1	0	1

(b)

Fig. 1. (a) Analog front-end. (b) Truth table of Qhp, Qhn, Qlp and Qln @ Ck is high.

II. Analog Front-End

Fig. 1 shows the analog front-end of the PAM-4 receiver. It is composed of two comparators, CMPH and CMPL, and the proposed MTIL. The comparators are realized by a four-input Strongarm latch. The input data D_{IN} is compared with two reference voltages V_{RH} and V_{RL}. When the clock CK is low, four outputs, Q_{HP}, Q_{HN}, Q_{LP} and Q_{LN}, are pre-charged to high. When CK goes high, these four outputs versus D_{IN} are listed in Fig. 1. By combining with the MTIL outputs, the data recovery and the phase detection will be completed.

A. Operation of MTIL

Before explaining the operation of the MTIL, let us consider the four-input Strongarm latch in Fig. 2 [11]. It is composed of two differential pairs, $M_1 \sim M_4$, a latch, $M_5 \sim M_8$, two offset-calibrating transistors, M_{N1} and M_{N2}, and five transistors driven by CK. When CK is low, two outputs, Q_P and Q_N, are pre-charged to high. When CK goes high, the total delay t_d [11] of the Strongarm latch is given as

$$t_d = t_{dis} + t_{latch} \quad (1)$$

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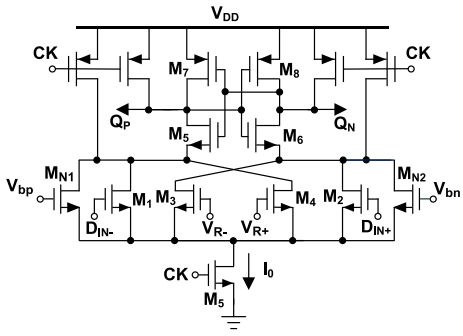


Fig. 2. Four-input Strongarm latch.

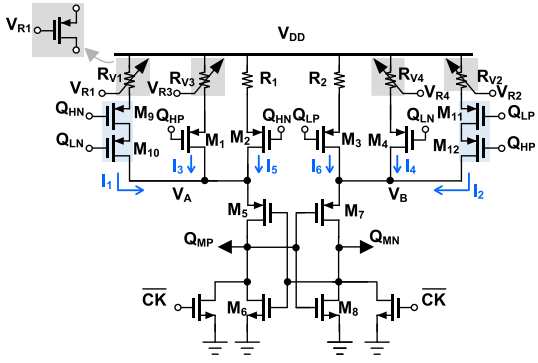


Fig. 3. The proposed MTIL.

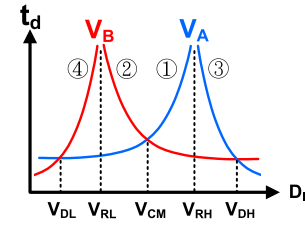


Fig. 4. The total delay time from D_{IN} to V_A and V_B versus D_{IN}.

where t_{dis} represents the capacitive discharge time of the load capacitance C_L at both Q_P and Q_N. It is given as

$$t_{dis} = \frac{2C_L}{I_0}|V_{thp}| \tag{2}$$

where the current I_0 is provided by M_5 after CK goes high and V_{thp} is the threshold voltage of a PMOS transistor. The delay time t_{latch} [11] is expressed as

$$t_{latch} = \frac{C_L}{g_m}\ln\left(\frac{\alpha}{\Delta V_{IN}}\right) \tag{3}$$

where g_m is the effective transconductance of $M_{P1}\sim M_{P4}$, ΔV_{IN} ($=D_{IN+}$-D_{IN-}-V_{R+}+V_{R-}) is the input voltage difference, $\alpha = \frac{0.5V_{DD}-|V_{thp}|}{|V_{thp}|}\cdot\sqrt{\frac{I_0}{2\beta}}$, V_{DD} is the supply voltage, and β is the transconductance parameter.

The proposed MTIL is shown in Fig. 3. When CK is low, the outputs, Q_{MP} and Q_{MN}, are discharged to low. When CK goes high, the operation of the MTIL depends upon Q_{HP}, Q_{HN}, Q_{LP}, and Q_{LN}. It is important to balance the capacitive loadings for four outputs of Strongarm latches. For $M_9 \sim M_{12}$ in Fig. 3, each PMOS transistor is split into two ones with a half of the aspect ratio.

According to Fig. 1, D_{IN} is divided into three regions and the operation of the MTIL is described as follows. In the first region, when $V_{RH} > D_{IN} > V_{RL}$, Q_{HP}=Q_{LN}=0 and Q_{HN}=Q_{LP}=1 are given in Fig. 1. The currents I_1, I_2, I_5, and I_6 are turned off. The voltages V_A and V_B are charged by the currents I_3 and I_4, respectively. Assume the average current I_3 charges V_A to turn on M_5 with the charging time t_{chg}, which is expressed as

$$t_{chg} = \frac{C_{LA}}{I_3}|V_{thp5}| \tag{4}$$

where V_{thp5} is the threshold voltage of M_5 and C_{LA} is the load capacitance at the source of M_5. By using (2)∼(4), the total delay time t_{d1} from D_{IN} to V_A is given as

$$t_{d1} = t_{dis} + \frac{C_L}{g_m}\ln\left(\frac{\alpha}{V_{RH}-D_{IN}}\right) + \frac{C_{LA}}{I_3}|V_{thp5}| \tag{5}$$

Fig. 4 shows the total delay time from D_{IN} to V_A and V_B versus D_{IN}, respectively, where the curve ① represents t_{d1}. Similarly, I_4 charges V_B to turn on M_7. The total delay time t_{d2} from D_{IN} to V_B is expressed as

$$t_{d2} = t_{dis} + \frac{C_L}{g_m}\ln\left(\frac{\alpha}{D_{IN}-V_{RL}}\right) + \frac{C_{LB}}{I_4}|V_{thp7}| \tag{6}$$

where V_{thp7} is the threshold voltage of M_7 and C_{LB} is the load capacitance at the source of M_7. In Fig. 4, the curve ② represents t_{d2}. Assuming $I_3 = I_4$, $C_{LA} = C_{LB}$, and V_{thp5}=V_{thp7}, the curves ① and ② intersect at $D_{IN} = \frac{V_{RH}+V_{RL}}{2}$ where $\frac{V_{RH}+V_{RL}}{2}$ is defined as the common-mode voltage V_{CM}. When V_{RH}>V_{CM}>D_{IN}>V_{RL}, one can find $t_{d1} < t_{d2}$. It leads to V_A rising faster than V_B and Q_{MP} is charging faster than Q_{MN}. The MTIL will output $Q_{MP} = 1$ and Q_{MN}=0. Similarly, if V_{RH}>D_{IN} >V_{CM} >V_{RN}, $t_{d1} > t_{d2}$ and V_A rises slower than V_B. It leads to $Q_{MP} = 0$ and Q_{MN}=1. Note that the MTIL equivalently determines the comparison result of D_{IN} and V_{CM}.

In the second region, when $D_{IN} > V_{RH}$, Q_{HP}=Q_{LP}=1 and Q_{HN}= Q_{LN}=0 and the currents I_2, I_3, and I_6 are turned off. The average currents I_1 and I_5 charge V_A to turn on M_5. From D_{IN} to V_A, the total delay time t_{d3} is given as

$$t_{d3} = t_{dis} + \frac{C_L}{g_m}\ln\left(\frac{\alpha}{D_{IN}-V_{RH}}\right) + \frac{C_{LA}}{I_1+I_5}|V_{thp5}| \tag{7}$$

In Fig. 4, the curve ③ represents t_{d3} and the curves ② and ③ intersect at D_{IN}=V_{DH}. Assume $C_{LA} = C_{LB} = C_{L2}$ and V_{thp5}=V_{thp7} = V_{thp}. Note that the curve ② is described by (6). According to (6) and (7), V_{DH} is derived as

$$V_{DH} = V_{RH} + \frac{V_{RH}-V_{RL}}{e^{g_m\left(\frac{C_{L2}}{C_L}\right)|V_{thp}|\left(\frac{1}{I_4}-\frac{1}{I_1+I_5}\right)}-1} \tag{8}$$

When $V_{DH} > D_{IN} > V_{RH}$ or D_{IN} >V_{DH}, t_{d2} is less or larger than t_{d3}, respectively. Since V_A rises slower or faster than V_B, Q_{MP}/Q_{MN} are equal to 0/1 or 1/0, respectively. Note that the MTIL equivalently determines the comparison result of D_{IN} and V_{DH} in this region.

In the third region, when D_{IN} <V_{RL}, Q_{LN}=Q_{HN}=1 and Q_{LP}= Q_{HP}=0, the currents I_1, I_4, and I_5 are turned off. The total delay time t_{d4} from D_{IN} to V_B is expressed as

$$t_{d4} = t_{dis} + \frac{C_L}{g_m}\ln\left(\frac{\alpha}{V_{RL}-D_{IN}}\right) + \frac{C_{LB}}{I_2+I_6}|V_{thp7}| \tag{9}$$

TABLE II
THE TRUTH TABLE OF ANALOG FRONT-END IN FIG. 1

Region	Q_{HP}	Q_{HN}	Q_{LP}	Q_{LN}	Q_{MP}	Q_{MN}	$*Q_{CM}$	Recovered Symbol
$D_{IN}>V_{DH}$	1	0	1	0	1	0	1	+3
$V_{DH}>D_{IN}>V_{RH}$	1	0	1	0	0	1	1	+1
$V_{RH}>D_{IN}>V_{CM}$	0	1	1	0	0	1	1	
$V_{CM}>D_{IN}>V_{RL}$	0	1	1	0	1	0	0	-1
$V_{RL}>D_{IN}>V_{DL}$	0	1	0	1	1	0	0	
$D_{IN}<V_{DL}$	0	1	0	1	0	1	0	-3

$*Q_{CM}=Q_{LP}(Q_{MN}+Q_{HP})$

In Fig. 4, the curve ④ represents t_{d4} and the curves ① and ④ intersect at V_{DL}. Note that the curve ① is described by (5).

According to (5) and (9), V_{DL} is derived as

$$V_{DL} = V_{RL} - \frac{V_{RH} - V_{RL}}{e^{g_m\left(\frac{C_{L2}}{C_L}\right)|V_{thp}|\left(\frac{1}{I_3} - \frac{1}{I_2+I_6}\right)} - 1} \tag{10}$$

When $V_{DL} < D_{IN} < V_{RL}$ or $D_{IN} < V_{DL}$, t_{d1} is less or larger than t_{d4}, respectively, and Q_{MP}/Q_{MN} are equal to 1/0 or 0/1. Based on the above discussions, Q_{MP} is summarized as

$$Q_{MP} = \begin{cases} 0, & \text{if } D_{IN} < V_{DL} \text{ or } V_{DH} > D_{IN} > V_{CM} \\ 1, & \text{if } D_{IN} > V_{DH} \text{ or } V_{CM} > D_{IN} > V_{DL}. \end{cases} \tag{11}$$

where Q_{MN} is equal to the inverse of Q_{MP}. In summary, the relation among Q_{HP}, Q_{HN}, Q_{LP}, Q_{LN}, Q_{MP} and Q_{MN} is listed in Table II.

In Fig. 3, the variable resistors R_{v1}, R_{v2}, R_{v3} and R_{v4} are realized by PMOS transistors. The resistors R_1 and R_2 are also realized by the PMOS transistors to match R_{v3} and R_{v4}, respectively. However, the undesired passive/active device mismatches (e.g., R_{V3} and R_{V4}) may alter the intersecting voltages V_{DL}, V_{CM}, and V_{DH}, which degrade the MTIL's accuracy. The variable resistors in the MTIL will be calibrated which will be discussed in Section III. Note that it equivalently calibrates V_{DL}, V_{CM}, and V_{DH}.

B. Data Recovery and Phase Detection

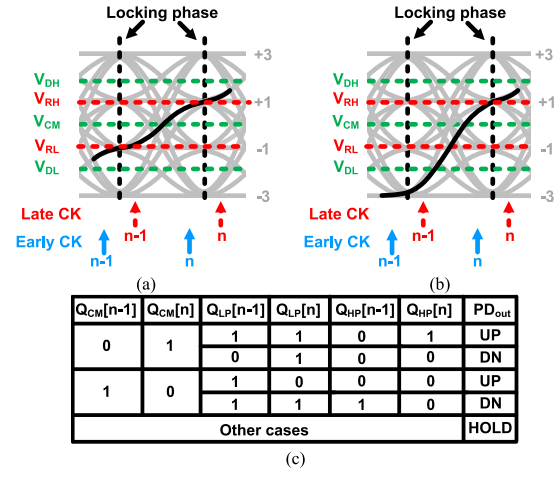
To explain the data recovery, let us consider the PAM-4 eye diagram in Fig. 5(a). The PAM-4 data are recovered by comparing D_{IN} with V_{DH}, V_{CM} and V_{DL}, respectively. The corresponding recovered symbols, +3, +1, −1 and −3, are also shown in Table II.

To explain the phase detection, a logic variable Q_{CM} is defined to be $Q_{LP}(Q_{MN}+Q_{HP})$ and its truth table is also listed in Table II. The relation among Q_{CM}, D_{IN}, and V_{CM} is given as

$$Q_{CM} = \begin{cases} 0, & \text{if } D_{IN} < V_{CM} \\ 1, & \text{if } D_{IN} > V_{CM}. \end{cases} \tag{12}$$

When two consecutive symbols have a transition across V_{CM}, two consecutive Q_{CM} with {Q_{CM}[n-1], Q_{CM}[n]} of {0,1} or {1,0} are obtained where n is the index.

In this brief, two consecutive symbols of (−1,+1), (+1, −1), (−1,+3), (−3,+1), (+1, −3), and (+3,-1) are used for phase detection. To simplify the explanation, only two consecutive symbols (−1,+1) and (−3,+1) are discussed here. Fig. 5(a) shows two consecutive symbols of (−1,+1) with the black line. When CK is late, {Q_{CM}[n-1], Q_{CM}[n], Q_{LP}[n-1], Q_{LP}[n], Q_{HP}[n-1], Q_{HP}[n]}={0, 1, 1, 1, 0, 1} is obtained. The output PD_{out} of the baud-rate PD logic gives UP to speed the clock. When CK is early, {Q_{CM}[n-1], Q_{CM}[n], Q_{LP}[n-1], Q_{LP}[n], Q_{HP}[n-1], Q_{HP}[n]}={0, 1, 0, 1, 0, 0} is obtained and PD_{out} gives DN to slow down the clock. Fig. 5(b) shows two consecutive symbols of (−3,+1) with the black line. When {Q_{CM}[n-1], Q_{CM}[n], Q_{LP}[n-1], Q_{LP}[n], Q_{HP}[n-1], Q_{HP}[n]}={0, 1, 0, 1, 0, 0} is obtained, PD_{out} gives DN to slow down the clock. Fig. 5(c) shows the truth table of this baud-rate PD logic.



Q_{CM}[n-1]	Q_{CM}[n]	Q_{LP}[n-1]	Q_{LP}[n]	Q_{HP}[n-1]	Q_{HP}[n]	PD_{out}
0	1	1	1	0	1	UP
		0	1	0	0	DN
1	0	1	0	0	0	UP
		1	1	1	0	DN
Other cases						HOLD

(c)

Fig. 5. The PAM-4 eye diagram with two consecutive symbols of (a) (−1,+1), (b) (−3,+1), and (c) Truth table of the baud-rate PD logic.

III. CIRCUIT DESCRIPTION

Fig. 6 shows the proposed quarter-rate PAM4 receiver. It consists of a single-stage CTLE, 8 comparators, 4 MTILs, 12 Set-Reset (SR) latches, 24 resistor digital-to-analog converters (RDACs), 12 1:8 demultiplexers (DMUXs), a digitally-controlled oscillator (DCO), a divide-by-8 divider, and a synthesized logic. The CTLE [12] is composed of a differential amplifier with the degenerative resistor and capacitor. Its simulated boost gain is 3.6 dB at 12GHz. A common-mode feedback (CMFB) circuit [13] with the reference voltage $V_{CM,R}$ is used to stabilize the CTLE's output common-mode voltage.

The VCO generates the quadrature clocks, CKx, where x=0, 90, 180, and 270. A resistor ladder is shared by these 24 RDACs and each RDAC has an independent switch array. The thermometer codes $C_{H,i}$[15:0] and $C_{L,i}$[15:0] control the comparators to reduce the offset voltages, where i=0∼3. The binary codes $C_{V1,i}$[5:0]∼ $C_{V4,i}$[5:0] calibrate the MTILs, where i=0∼3. The synthesized logic is composed of an offset calibration logic, three binary-to-thermometer (B2T) converters, a data decoder logic, a PRBS checker [14], the baud-rate PD logic, and a first-order 10-bit digital loop filter (DLF). The calibrations for Strongarm latches and MTILs are discussed as follows.

A. Offset Calibration for Strongarm Latches

To calibrate the offset of the four-input Strongarm latch [6] in Fig. 2, the RDAC in Fig. 7(a) is used which is controlled by the thermometer code $C_{H,1}$[15:0]. The RDAC generates the voltages V_{bp} and V_{bn} to bias M_{N1} and M_{N2} in Fig. 2. Fig. 7(b) shows the offset calibration circuit. Four inputs of the comparator are shorted to the common-mode reference voltage $V_{CM,R}$. When the divide-by-8 clock $CK_{/8}$ goes high, the calibration logic determines the bit $C_{H,1}$ [15] and increases the code $C_{H,1}$[14:0] to raise V_{bp} or V_{bn}. Once the polarity

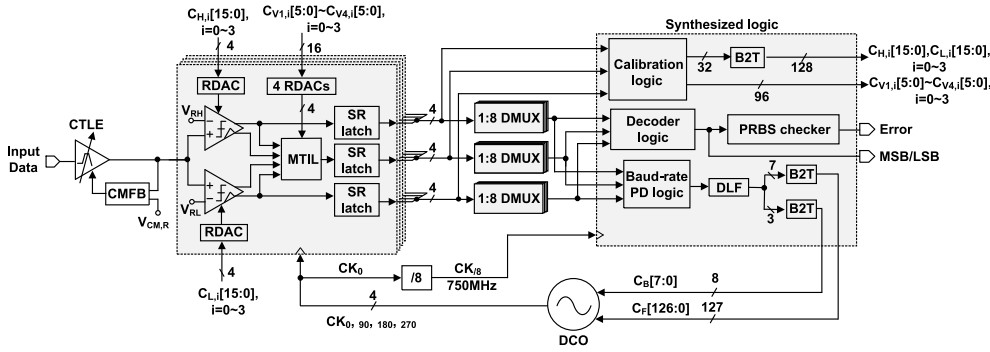


Fig. 6. The proposed quarter-rate PAM-4 receiver.

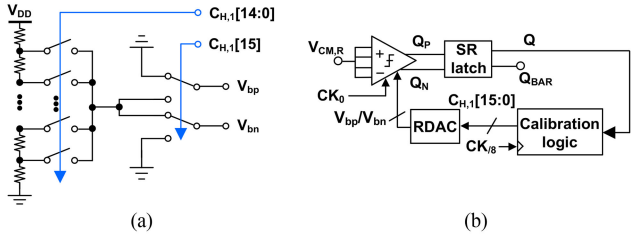


Fig. 7. (a) RDAC and (b) offset calibration circuit.

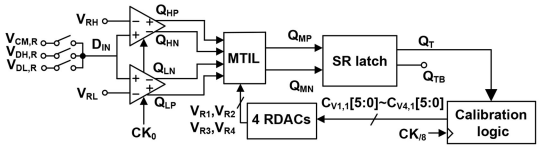


Fig. 8. Calibration circuit for the MTIL.

of Q is changed, the calibration is finished and $C_{H,1}[15:0]$ is stored.

B. Calibration for MTILs

The calibration circuit for the MTIL is shown in Fig. 8. Five reference voltages $V_{DH,R}$=920mV, V_{RH}=860mV, $V_{CM,R}$=800mV, V_{RL}=740mV and $V_{DL,R}$=680mV are used, where $V_{DH,R} > V_{RH} > V_{CM,R} > V_{RL} > V_{DL,R}$. It aims to calibrate the MTIL to achieve three intersecting voltages V_{CM}=$V_{CM,R}$, V_{DH}=$V_{DH,R}$ and V_{DL}=$V_{DL,R}$ in Fig. 4. First, D_{IN} is shorted to $V_{CM,R}$. According to Table II, one can find V_{HP}=V_{LN}=0 and V_{HN}=V_{LP}=1. Then, both the currents I_3 and I_4 of the MTIL are turned on. When $CK_{/8}$ goes high and assume that the initial value of Q_T=1, the calibration logic increases the binary code $C_{V3,1}[5:0]$ to raise V_{R3}. Once Q_T turns to 0, the calibration is finished and $C_{V3,1}[5:0]$ is stored. While the initial value of Q_T=0, $C_{V4,1}[5:0]$ is increased to raise V_{R4} until Q_T =1. Thus, the intersecting voltage V_{CM}=$V_{CM,R}$ is calibrated. Similarly, to calibrate V_{DH} and V_{DL}, D_{IN} is shorted to $V_{DH,R}$ and $V_{DL,R}$, respectively. The calibration logic generates $C_{V1,1}[5:0]$ and $C_{V2,1}[5:0]$ to have V_{DH} =$V_{DH,R}$ and V_{DL} =$V_{DL,R}$, respectively. The remaining MTILs are calibrated by the same way. Finally, the calibrations for the comparators and MTILs are executed twice alternatively.

C. DCO

Fig. 9(a) shows the DCO which is composed of a two-stage voltage-controlled oscillator (VCO) [15], a RDAC, and aPMOS array. Fig. 9(b) shows the delay cell. It is composed of

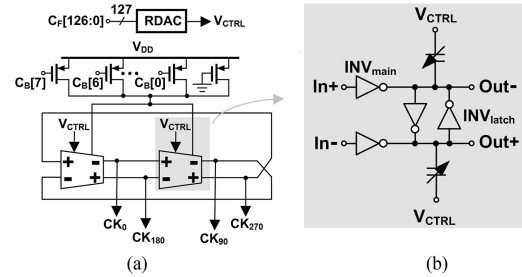


Fig. 9. (a) DCO and (b) its delay cell.

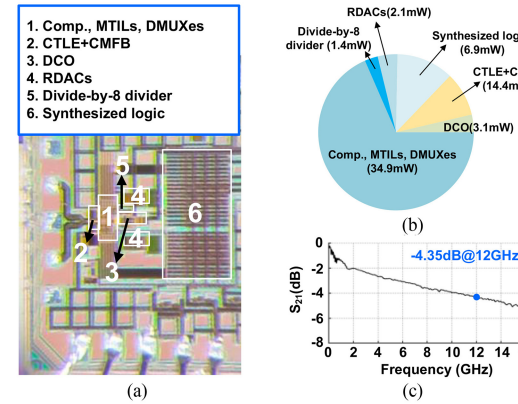
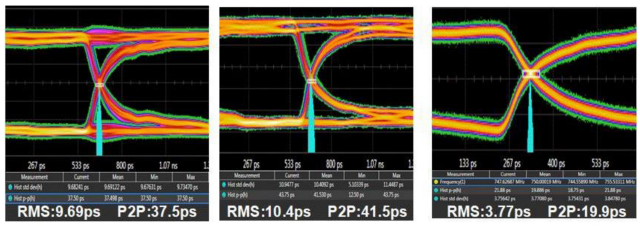


Fig. 10. (a) Die photo, (b) power breakdown, and (c) measured channel response.

two main inverters INV_{main}, two latch inverters INV_{latch}, and two varactors. The ratio of INV_{latch} and INV_{main} is equal to 0.7 [15]. The output thermometer codes $C_B[7:0]$ and $C_F[126:0]$ of the DLF adjust the DCO's frequency. The simulated phase noise of the VCO operated at 6-GHz is −83 dBc/Hz at the 1MHz offset frequency and its frequency range is from 4.8 to 7.4GHz.

IV. Experimental Results

This 48-Gb/s PAM4 receiver is fabricated in a 40-nm CMOS process. Fig. 10(a) shows the die photo with the active area of 0.089mm^2. Fig. 10(b) shows the power breakdown of this PAM-4 receiver. The total power is 62.8mW and the calculated energy efficiency is 1.31pJ/bit. Fig. 10(c) shows the measured frequency response of the channel with the loss of −4.35dB at 12GHz. Using a pseudo random bit sequence (PRBS) of 2^7-1, Fig. 11(a) shows the eye diagrams of the most-significant-bit (MSB) of the recovered data de-serialized by 32 at 750Mb/s with the bit error rate (BER)<10^{-12}. Its measured root-mean-square (RMS) and peak-to-peak jitter is 9.69ps and 37.5ps,



(a) (b) (c)

Fig. 11. Measured eye diagrams of (a)MSB, (b) LSB of the recovered data de-serialized by 32 at 750Mb/s, and (c) divide-by-8 recovered clock of 750MHz.

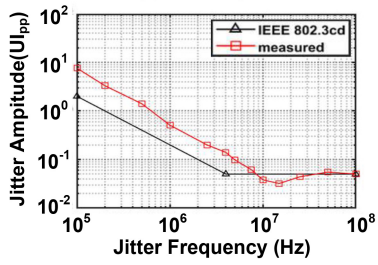


Fig. 12. Measured JTOL with BER<10^{-12}.

respectively. Fig. 11(b) shows the eye diagrams of the least-significant-bit (LSB) of the recovered data de-serialized by 32 at 750Mb/s with the BER < 10^{-12}. Its RMS and peak-to-peak jitter is 10.4ps and 41.53ps, respectively. Fig. 11(c) shows the measured divide-by-8 recovered clock of 750MHz. Its RMS and peak-to-peak jitter is 3.77ps and 19.9ps respectively. Fig. 12 shows the measured jitter tolerance (JTOL) with the BER<10^{-12}. The measured lowest JTOL is 0.032UIpp at 15MHz. The long latency of this digital CDR leads to the accumulated phase error which degrades the JTOL performance. When the PRBS of 2^{11}-1 and 2^{31}-1 is used, the measured BER is around 10^{-9} and 10^{-3}, respectively. The performance summary and the comparison are listed in Table III. This PAM-4 receiver has the least number of input comparators, compared with [4], [5], [10], [16], [17]. Compared to the Strongarm latch, the MTIL needs more transistors, but no tail transistor driven by the clock is used. It reduces the power of the clock buffer. In addition, the analog front-end of this brief adopts two comparators and one MTIL which need the cross-coupled latches to latch data. It also has the advantage with few latches. Compared with [10], this brief can detect the same number of transition density using the less comparators.

V. Conclusion

The quarter-rate PAM-4 receiver with the MTILs is presented. The number of input comparators is reduced which relaxes the capacitive loadings for the CTLE and improves the energy efficiency. The proposed MTIL relies on the time difference to determine the comparison results. However, when the channel loss increases, the undesired channel ISI and the time-domain jitter will degrade the BER.

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TABLE III
Performance Summary and Comparison of PAM-4 CDRs

	[4]	[5]	[10]	[16]	[17]	**Our**
Technology	40 nm	28 nm	7 nm	65 nm	28 nm	**40 nm**
Chan. Loss (dB)	4	7.1	17.8	20.8	N/A	**4.35**
Data Rate [Gb/s]	48	52	56.25	56	47.6-58.8	**48**
# of Comp. @ full rate	5	4	4	5	4	**2**
PD type	Baud-rate	Baud-rate	Over-sampling	Over-sampling	Over-sampling	**Baud-rate**
RMS jitter(ps) @ clock freq.(Hz)	N/A	0.48 @3.25G	N/A	N/A	0.533 @13G	**3.77 @750 M**
JTOL(UI_{PP}) @ jitter freq.(Hz)	0.08 @250M	0.1 @100M	0.12 @10M	0.12 @100M	0.1 @100M	**0.032 @15M**
BER	< 10^{-11}	< 10^{-12}	< 10^{-12}	< 10^{-12}	< 10^{-12}	**< 10^{-12}**
Power [mW]	116.3	43.1	79	259	11-13.1	**62.8**
Area [mm^2]	0.24	0.011	0.13	0.51	0.056	**0.089**
FoM (pJ/b)	2.42	0.83	1.41	4.63	0.22-0.25	**1.31**

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